REMARKS

Claims 1-25 are pending in this application. Claims 1, 8, 13, and 20 been amended to clarify the preamble and not for narrowing purposes.

The Office Action rejected claim 3 under 35 U.S.C. 112 as being indefinite for not defining the recited overlapping functions. Applicant respectfully traverses this rejection. The overlap functions: AVERAGE; MAX, ADD, and TOP are well-known terms that are defined in dictionaries and in the specification of the subject patent application. Moreover, there is no requirement that claim terms be defined in the claims. The AVERAGE function is discussed at page 4, lines 15-20 of the specification. The MAX function is discussed at page 4, line 21- Page 5, line 9 of the specification. The ADD function is discussed at page 3, line 22 – page 4, line 7 of the specification. The TOP function is discussed at page 6, lines 1-12 of the specification.

The Office Action rejected claims 1-19 under 35 U.S.C. 102(e) as being anticipated by Bergstrom (U.S. 6,801,213, hereafter "Bergstrom"). The Office Action did not reject or comment on claims 20-25. Applicant respectfully traverses the rejection.

Claim 1 reads as follows:

"A method for transforming multiple one-bit per pixel images for presentation on a device, comprising steps of: a) converting the one-bit per pixel images to multiple bits per pixel images; b) overlapping the multiple bits per pixel images, according to an overlap function, to create a composite multiple bits per pixel image; c) converting the composite multiple bits per pixel image into a dithered one-bit per pixel image by applying a spatial dithering algorithm; and d) presenting the dithered one-bit per pixel image on a display."

I. Bergstrom neither teaches nor suggests the claimed step of "converting the one-bit per pixel images to multiple bits per pixel images." The Office Action cited col. Col. 5, lines 13-20; col. 15, lines 1-10 and 29-41; col. 20, line 65 – col. 21, line 15; and col. 3, lines 18-28.

Col. 5, lines 13-20, reads:

"A display matrix is provided for forming a composite image from a series of sub-images. In general, the display matrix includes a plurality of display elements, each display element including a pixel, and a display circuit electrically connected to the pixel. Each display circuit includes a plurality of memory cells, and a selector for outputting to the pixel data from one memory cell at a time."

Col. 15, lines 1-10 and 29-41 read:

"By displaying each bit for different portions of the time that a particular frame is displayed, a multiple grayscale field may be formed. One bit may be displayed for a larger portion of the time that a particular frame is displayed either by displaying that bit longer, as illustrated in FIG. 9A, or by displaying that bit more frequently, as illustrated in FIG. 9B. For example, a four-level grayscale system is achieved in a two bit system when the MSB sub-image is displayed for twice as long as the LSB sub-image. The total display time for both sub-images equals the display time for the field.

In one embodiment of the present invention, two memory cells are present in each display circuit. Once data has been loaded into the display matrix, it is possible to form either a dichromic composite static image or a four-level grayscale monochromic composite static image. In the dichromic case, one memory cell of each display circuit contains the data corresponding to one color field and to the location of the display circuit within the image. The second memory cell contains the corresponding data for the second field. By cycling between the two sub-images corresponding to the memory cells within each display element, a dichromic composite static image is formed."

Col. 20, line 65 – col. 21, line 15 read:

"Modes of Operating the Display Matrix

Several different modes for operating a display matrix according to the present invention are possible. One mode, referred to herein as the 'Power Miser Mode,' relates to a mode where writing to the display matrix is minimized, there reducing the amount of energy consumed by the display matrix. Another mode of operation, referred to herein as the 'Color Rich Mode,' relates to a mode where data is written to memory cells forming one bit plane while memory cells of another bit plane are used to display an image in order increase the number of sub-

images that can be used to form a composite image. By being able to increase the number of sub-images that can be used to form a composite image, a greater number of colors may be formed by the display matrix. Yet another mode of operation, referred to herein as the 'Color Mixing Mode,' involves operating a display matrix in a Power Miser Mode and Color Rich Mode at the same time."

Col. 3, lines 18-28 reads:

"As was noted above, most displays must be frequently rewritten to maintain an image. In the case of both CRT and AMLCD displays, data is being rewritten to one part of the display area while the rest of the array continues to display the prior image frame. This property is particular to monochrome displays and to color images are created from a composite of spatially separated sub-pixels. There is a clear advantage to writing and displaying data at the same time allowing each function to make maximum utilization of time allowed for each frame."

None of the above-quoted parts (or any other parts) of Bergstrom teach or suggest the *conversion* of an image using single-bit pixels into an image with multiple bits per pixel. Bergstrom relates to methods for applying digital information to generate color and grayscale images. See col. 1, lines 14-16. Nowhere in the cited parts of Bergstrom is there any discussion of single bit pixel images being converted to multiple-bit pixel images, as claimed. Rather Bergstrom appears concerned with the timing of the display of images to achieve certain effects that have nothing whatsoever to do with Applicant's claimed invention. Thus, Bergstrom discusses forming composite images from sub-images and display elements, each comprising a pixel and not bit-per pixel images or multiple bits per pixel images.

II. Bergstrom neither teaches nor suggests the claimed step of "overlapping the multiple bits per pixel images, according to an overlap function, to create a composite multiple bits per pixel image." The Office Action cited col. 5, lines 13-20; col. 15, lines 1-10 and 29-41; col. 20, line 65 – col. 21, line 15; and col. 3, lines 18-28. These are the same parts of Bergstrom cited for the first step of claim 1. None of the cited parts of Bergstrom teach or suggest using an overlapping function to overlap the composite multiple bit per pixel images. While Bergstrom discusses composite images (see col. 5, lines 13-20), nowhere does it teach a

composite image as claimed. Bergstrom at col. 3, lines 26-27 discusses "writing and displaying data at the same time" and not overlapping different images at the same time. While Bergstrom discusses circuits overlapping each pixel (col. 20, line 55), it does not discuss overlapping the images as claimed, nor does it discuss the use of an overlap function as also claimed. At the cited col. 23, line 58-col. 24, line 60, Bergstrom discusses strobing algorithms to achieve certain gray levels. That has nothing to do with the claimed invention where images are overlapped, not strobed.

III. Bergstrom neither teaches nor suggests the claimed step of "converting the composite multiple bits per pixel image into a dithered one-bit per pixel image by applying a spatial dithering algorithm." The Office Action cited col. 25, line 66 – col. 26, line 18; col. 23, line 58-col. 24, line 60; and col. 25, line 67 – col. 26, line 18.

Col. 23, line 58-col. 24, line 60, reads:
"Various strobing algorithms are possible to achieve a certain gray level. For instance, in a 3 bit-plane system, a conventional coding scheme might divide up an interval, such as the RECOVERY or ACTIVE period, into seven equal parts, and assign the MSB plane to the first four parts, the SSB plane to the next two parts, and the LSB plane to the last part. Then a gray level 4 would be achieved by a 1111000 sequence, a 5 by a 1111001 sequence, etc.

One algorithm that has been found empirically to have a better RMS effect than the above conventional coding scheme for a particular LCD is called distributed binary coding. A better RMS effect refers to the gradation in voltages driven on the liquid crystal being more uniform. The strobing formula for distributed binary coding is {MSB, SSB, MSB, LSB, MSB, SSB, MSB}. For example, 0={0000000}, 1={0001000}, 2={0100010}, 3={0101010}, 4={1010101}, 5={1011101},. 6={1110111}, and 7={1111111}. In FIG. 18, distributed binary coding is used to display a grayscale 3 in the red field followed by a 6 in the green field.

While the above formula relates to the present invention with three bit planes, distributed binary coding can be extended to display matrices of any number N of bit planes. The interval is first always divided into (2.sup.N- 1) time slots. The MSB plane time slots are

determined first. The MSB plane is always placed in the first time slot and every other time slot there after. The 2.sup.nd SB plane time slots is calculated next. The SSB plane is placed in the first available time slot and every fourth time slot thereafter. The 3.sup.rd SB occupies the next available time slot and every eighth slot thereafter, and so on until the LSB (N.sup.th) plane is place in the middle time slot. For instance, for four bit planes, the formula is {MSB, 2.sup.nd SB, MSB, 3.sup.rd SB, MSB, 2.sup.nd SB, LSB, MSB, 3.sup.rd SB, MSB, 2.sup.nd SB, MSB}.

The ability of the display system of the present invention to perform distributed binary coding is a strong example of one of the advantages that the display circuit of the present invention provides. The grayscale level is strobed twice in one color field, once in the RECOVERY period and once in the ACTIVE period, for a total of 14 time slots. In a system with only one memory cell per display circuit, fourteen bit planes would have to be loaded in order to strobe during 14 different time slots. This would require a very high bandwidth transfer rate and pixel refresh rate. However, by using a display matrix capable of storing three different bit planes, different bit planes need not be continuously written into a display matrix. This allows strobing the transition between strobing different bit planes to be significantly reduced, thereby making it possible to have 14 time slots.

According to the present invention, it is possible to alternate the assignment of MSB memory matrices for consecutive color fields. This enables the display matrix to further take advantage of having more than one memory cell in each display circuit. For instance, in the above sequence, the {RED, GREEN, BLUE} memory matrices were assigned to {MSB, SSB, LSB} for the RED field, while in the ensuing GREEN field, the assignments were switched to {LSB, SSB, MSB}. This algorithm is driven by the nature of distributed binary coding, in which the LSB plane always falls in the middle time slot while the MSB plane is always at the beginning. Once the LSB plane for the ACTIVE period of the RED field has completed, the memory plane can be used for the first plane needed by the GREEN field, which is the MSB plane. Hence, by modifying the assignment of the bit planes as MSB, SSB and LSB, etc., it is possible to increase the number of bit planes which can be written to memory and strobed.

Distributed binary coding and the accompanying strategies discussed above have been found empirically preferable for certain liquid crystal formulations. Other algorithms may be better suited for other display matrices and are intended to fall within the scope of the present invention."

Col. 25, line 67 – col. 26, line 18, read:
"The hardware and software work together in combination with the algorithms of the present invention.

In separating and storing color data, various types of image processing, such as spatial dithering, may be applied to the data either before or after the image data is separated into the color fields. This storage can either take place within the ASIC chip 802 or on a separate frame buffer chip 808 (memory) connected to the ASIC.

A second feature of the ASIC 802 is its ability to rapidly send each color field to the backplane 806 in a specific sequence as may be required for a given algorithm. As is described herein, the algorithms of the present invention involve different applications of individual bits of color field data, depending on the method. These various methods have been optimized for color generation under various device designs, environmental conditions and color requirements, and refresh rates. Data transfer bit sequencing, timing and clock speeds can be set by the ASIC chip."

Although, Bergstrom discusses spatial dithering (col. 26, line 4), that discussion is in the context of separating bit-mapped data into separate color components (see col. 25, lines 52-60) and not to convert the composite images to dithered one-bit per pixel images, as claimed.

IV. Bergstrom neither teaches nor suggests the claimed step of presenting the dithered one-bit per pixel image on a display. Specifically, nowhere in Bergstrom is a teaching of displaying dithered one-bit per pixel image. Instead, the cited parts of Bergstrom discuss display of each bit at different portions of time (col. 15, lines 1-10) and writing and displaying data at the same time Col. 3, lines 18-28).

V. Claims 2-7 depend on claim 1 and are patentable for the reasons discussed herein with respect to claim 1. Claim 13 is an apparatus counterpart of claim 1 and it and its dependent claims are patentable for the reasons discussed herein with respect to claim 1.

VI. Claim 8 is an independent method claim that reads:
"A method for transforming multiple one-bit per pixel images for presentation on a device, comprising steps of: a) applying different stipple patterns to each of the one-bit per pixel images to create multiple stippled images; b) overlaying the stippled images to create a composite stippled one-bit per pixel image; and c) presenting the composite stippled one-bit per pixel image on a display."

Although the Office Action Summary and Paragraph 5 both state that claims 1-19 were rejected, there is no explanation of the rejection of claim 8. Therefore, the United States Patent and Trademark Office has not carried its burden of showing anticipation. Moreover, the undersigned has examined the Bergstrom patent and did not find a single reference to stippling, as required by claim 8. There cannot be any anticipation without a showing that each claimed element and limitation is present in a single prior art reference.

Applicant respectfully requests reconsideration of the rejections and allowance of the claims in view of the amendments and remarks made herein.

Respectfully submitted,

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